

[CONTROL CHIP WITH MUTLIPLE-LAYER DEFER QUEUE]

Abstract of Disclosure

A control chip having a multiple-layer defer queue therein and a method of operating the control chip. The control chip is coupled to a CPU bus and a PCI bus. The control chip comprises of a PC request queue, a multiple-layer defer queue, a PCI access queue and a PCI controller. The multiple-layer defer queue facilitates the processing of a multiple of concurrent CPU requests that belong to a first request type. The multiple-layer defer queue supports retry and defer transactions, thereby reducing data transmission between the CPU and the control chip.

Figures